Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	4	(("6121668") or ("6245600") or ("6413857") or ("20020132395")). PN.	US-PGPUB; USPAT	OR	OFF	2005/04/01 10:52
L10	1220	(SOI or (silicon adj on adj insulator)) and (ion adj beam)	US-PGPUB; USPAT	OR	ON	2005/04/01 12:53
L11	973	10 and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 12:54
L12	42	(buried adj oxide) same (ion adj beam)	US-PGPUB; USPAT	OR	ON	2005/04/01 12:49
L13	12	(buried adj oxide) and (ion adj beam)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/01 12:49
L14	84	(SOI or (silicon adj on adj insulator)) and (ion adj beam)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/01 12:51
L15	183	(ESD) and (ion adj beam)	US-PGPUB; USPAT	OR	ON	2005/04/01 12:53
L16	155	15 and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 12:59
L17	824	((break adj down) with (insulating or insulator or dielectric)) and (ion or beam or ionized) and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 13:27
L18	5	((break adj down) with (insulating or insulator or dielectric)) and (FIB) and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 13:10
L19	4	((break adj down) with (insulating or insulator or dielectric)) and (focused adj ion adj beam) and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 13:27
L21	0	((break adj down) with (insulating or insulator or dielectric)) and (focused adj ion adj beam)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/01 13:12
L22	0	((break adj down) with (SOI or (buried adj oxide))) and (focused adj ion adj beam)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/01 13:13
L23	1	((break adj down) with (SOI or (buried adj oxide))) and (focused adj ion adj beam)	US-PGPUB; USPAT	OR	ON	2005/04/01 13:13
L24	66	((break adj down) with (insulating or insulator or dielectric)) and (ion adj beam) and @ad<"20030219"	US-PGPUB; USPAT	OR	ON	2005/04/01 13:29

L25	3	((break adj down) with (insulating or insulator or dielectric)) and (ion adj beam)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/01 13:30

US-PAT-NO: 6197621

DOCUMENT-IDENTIFIER: US 6197621 B1

TITLE: Custom laser conductor linkage for integrated circuits

---------- KWIC ---------

Application Filing Date - AD (1):
19990618

Brief Summary Text - BSTX (7):
In an "antifuse" approach to electrically programming a circuit, a large voltage differential is applied across two adjacent conductors (on the same or different layers) so that the intervening **dielectric breaks down,** thus creating a link. A problem with the antifuse approach is that the resulting link has relatively high impedance, so large currents, e.g., driver currents, cannot be handled. Furthermore, the antifuse approach is limited to creating links, whereas it is desirable to be able to create reliable opens along existing conductors as well.

Brief Summary Text - BSTX (9):
Focused ion beam systems have been used to make connections as well as break them. A focused, rasterized beam of high-energy ions, e.g., gallium ions, can be used to sputter and remove dielectric over metal lines. If a break is desired, the beam can be used to precisely cut through the metal. If a new connection is desired between thus exposed conductors, the metal itself is left undisturbed; metal-bearing, e.g., tungsten carbonyl, gas is admitted into the vacuum chamber. The ion beam is scanned from one metal electrical node to the other. The ion beam locally decomposes the metal-bearing gas adsorbed onto the surface, leaving a conductive trace between the metal electrical nodes. This technique is very flexible, permitting connections even between nodes that are on the same or different metal interconnect levels and disposed far apart on the integrated circuit.

Brief Summary Text - BSTX (10):
The main advantage of the **focused ion beam** approach is that it allows flexible modification of an integrated circuit, both before and after integrated circuit manufacture is completed. The **focused ion beam** approach is costly in that the equipment is expensive and requires a high degree of skill

on the part of the operator. If circuit breaks are required in isolated lines, the laser cutting approach is most cost effective. However, as with laser cutting, the **focused ion beam** damages intermetal and passivation dielectric, the effects of which can be difficult to predict and control. Accordingly, devices so modified are best limited to design verification purposes; newly designed and manufactured devices are still required for end uses.

Brief Summary Text - BSTX (18):

The laser fusion method is less flexible than the **focused ion beam** in that the metal features to be linked must be close together and on the same metal layer. On the other hand, the equipment required for laser linking can cost an order of magnitude less than the equipment required for the **focused ion beam** method. Little training is required to operate the laser and there is no vacuum requirement. In the laser linkage approach, passivation and dielectric material is left in place; therefore exposure to moisture is minimized and no additional passivation steps are required to ensure long-term device reliability.

Detailed Description Text - DETX (25):

In addition, the present invention can be combined with **focused ion beam** techniques so that remote links can be formed. In this case, the laser link approach can reduce the number of connections that required the FIB technique, or laser linking can be used in conjunction with **focused ion beam** milling for device modification. Finally, the invention further provides for a variety of stages, microscopes, illumination systems and laser systems. In the latter case, a wide range of wavelengths can be used that are more readily absorbed by the metal than by the dielectric. These and other variations upon and modifications to the preferred embodiments are provided for by the present invention, the scope of which is limited only by the following claims.

US-PAT-NO: 6414335

DOCUMENT-IDENTIFIER: US 6414335 B1

TITLE: Selective state change analysis of a **SOI** die

---------- KWIC ---------

Abstract Text - ABTX (1):

Analysis of a semiconductor die having silicon-on-insulator (**SOI**) structure is enhanced by capacitively coupling a signal to the die. According to an example embodiment of the present invention, a die having a thinned back side is analyzed by capacitively coupling an input signal through the insulator portion of the **SOI** structure and effecting a state change to circuitry in the die. The state change is used to evaluate a characteristic of the die, such as by detecting a response to the state change. The ability to force such a state change is helpful for evaluating dies having **SOI** structure, and is particularly useful for evaluation techniques that require or benefit from maintaining the insulator portion of the **SOI** structure intact.

Application Filing Date - AD (1):

20010523

TITLE - TI (1):

Selective state change analysis of a **SOI** die

Parent Case Text - PCTX (2):

The Patent Document is related to U.S. patent application Ser. No. 09/864,665, entitled "Timing Margin Alteration Via the Insulator of a **SOI** Die," and to U.S. patent application Ser. No. 09/864,708, entitled "Logic State Mapping in a **SOI** Die," and both filed concurrently herewith.

Brief Summary Text - BSTX (8):

One particular type of semiconductor device structure that presents unique challenges to back side circuit analysis is silicon-on-insulator (**SOI**) structure. Forming a **SOI** structure involves forming an insulator, such as an oxide, over bulk silicon in the back side of a semiconductor device. A thin layer of silicon is formed on top of the insulator, and circuitry is formed over the insulator. The resulting **SOI** structure exhibits benefits including reduced switch capacitance, which leads to faster operation. Direct access to

circuitry for analysis of **SOI** structure, however, involves milling through the oxide. The milling process can damage circuitry or other structure in the device. Such damage can alter the characteristics of the device and render the analysis inaccurate. In addition, the milling process can be time-consuming, difficult to control, and expensive.

Brief Summary Text - BSTX (9):

One aspect of integrated circuit die operation that is important for analyzing dies involves the logic state of various circuitry in the die. Malfunctions or design problems are often related to certain circuitry that is not operating at the proper logic state, or is delayed in getting to or changing from a selected logic state. The detection of selected logic states is useful for various reasons, including determining whether a particular die is operating properly, and for isolating defects in a die. In **SOI** dies, detecting particular logic states can be difficult, however, for reasons including those stated hereinabove and related to the challenges presented to accessing circuitry in the die for such analysis.

Brief Summary Text - BSTX (10):

The difficulty, cost, and destructive aspects of existing methods for testing integrated circuits present challenges to the growth and improvement of semiconductor technologies involving **SOI** structure.

Brief Summary Text - BSTX (12):

The present invention is directed to a method and system for analyzing a semiconductor die having silicon-on-insulator (**SOI**) structure in a manner that addresses the above-mentioned challenges. The present invention is exemplified in a number of implementations and applications, some of which are summarized below.

Brief Summary Text - BSTX (13):

According to an example embodiment of the present invention, a semiconductor die having **SOI** structure and circuitry in a circuit side opposite a back side is analyzed. In a typical application, a portion of substrate is removed from the back side of the semiconductor die, and an electrical input is capacitively coupled through the insulator portion of the **SOI** structure. The input is selected to force a state change in circuitry in the die. For example, in one implementation, forcing a state change includes capacitively coupling a voltage to the circuitry and causing the circuitry to take on a selected state and/or isolating the circuitry. The resulting state change is used to evaluate a characteristic of the die.

Brief Summary Text - BSTX (14):

According to another example embodiment of the present invention, a system is adapted for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and circuitry in a circuit side opposite a back side. The system includes a probe adapted to capacitively couple an electrical input through the insulator portion of the SOI structure and selectively effect a state change to circuitry in the die. A detector is adapted to use the selected state change to evaluate a characteristic of the die.

Drawing Description Text - DRTX (3):

FIG. 1 is a semiconductor die having SOI structure and undergoing analysis, according to an example embodiment of the present invention;

Detailed Description Text - DETX (3):

The present invention is believed to be applicable to a variety of different types of semiconductor devices, and has been found to be particularly suited for flip-chips and other devices having silicon-on-insulator (SOI) structure and requiring or benefiting from analysis involving the operational state of a semiconductor die. While the present invention is not necessarily limited to such devices, various aspects of the invention may be appreciated through a discussion of various examples using this context.

Detailed Description Text - DETX (4):

According to an example embodiment of the present invention, a semiconductor die having SOI structure and a back side opposite circuitry in a circuit side is analyzed. The back side of the die is thinned, and an electrical input is capacitively coupled to a portion of the circuitry through the insulator of the SOI structure. The electrical input is directed to a portion of the die and forces selected circuitry to take on an electrical state. The input may include, for example, a charge coupled to the circuitry via an electron-beam probe and/or a signal coupled to the selected circuitry by isolating the circuitry from one or more other circuit components in the die. In the instance of an electron-beam probe, the application of the probe is selected to achieve a desired result, such as by raster scanning the probe across the die, stepping it across the die, pulsing it and/or directing it in a spot mode at a selected portion of the die.

Detailed Description Text - DETX (12):

FIG. 1 shows a portion of a flip-chip die 100 undergoing analysis, according to an example embodiment of the present invention. The die exemplifies one of a variety of dies having SOI structure for which the present invention is applicable. The die is in an inverted position with a circuit side 102 facing

down and a back side 104 facing up, such as would be a flip-chip die bonded to a package substrate. A portion of bulk silicon 110 in the back side has been removed to expose an insulating layer 120, such as a buried oxide (BOX) layer. The substrate removal is accomplished using a conventional method, such as by global thinning, local thinning or a combination thereof. The silicon substrate can be removed, for example, using commonly available substrate removal methods and devices, such as using a focused **ion beam** (FIB), a laser etching device, or an etch chamber having an etch gas and used in combination with a masking step. A thin layer of silicon 130, in combination with the insulator, forms a **SOI** structure. Source/drain regions 140 and 145 are located in the thin layer of silicon 130, and a gate 150 is located over the thin layer of silicon. The source, drain and gate make up a **SOI** transistor.

Detailed Description Text - DETX (17):

According to another example embodiment of the present invention, FIG. 4 shows a system 400 adapted to force a state change in a semiconductor die 405 having **SOI** structure. The system 400 includes a substrate removal device 450 adapted to remove substrate from a back side of the die and to form an exposed region. In one implementation, the substrate removal device includes a FIB, and in another implementation, the substrate removal device includes a laser-etching device. The die is positioned on a stage 410 and electrically coupled via the stage to an input device 430, such as a signal generator, adapted to power the die and obtain an electrical response from the die.

Claims Text - CLTX (1):

1. A method for analyzing a semiconductor die having silicon-on-insulator (**SOI**) structure and circuitry in a circuit side opposite a back side, the method comprising:

Claims Text - CLTX (2):

capacitively coupling an electrical input through the insulator portion of the **SOI** structure and selectively effecting a state change to circuitry in the die; and

Claims Text - CLTX (4):

2. The method of claim 1, further comprising thinning the back side of the die, and wherein capacitively coupling an electrical input includes directing an electron-beam probe at a selected portion of the thinned back side of the die to electrically couple a capacitance load to underlying circuitry via the insulator of the **SOI** structure and selectively effecting the state-change.

Claims Text - CLTX (6):

4. The method of claim 3, wherein isolating the circuitry includes milling through a portion of the insulator in the SOI structure, removing a portion of the circuitry and electrically isolating the circuitry.

Claims Text - CLTX (12):
10. The method of claim 1, wherein selectively effecting a state-change includes causing a source/drain region located in the SOI structure to change voltage.

Claims Text - CLTX (15):
13. The method of claim 1, wherein electrically coupling a capacitance load to underlying circuitry includes capacitively coupling through the insulator portion of the SOI and inducing a voltage upon the underlying circuitry.

Claims Text - CLTX (17):
15. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and circuitry in a circuit side opposite a back side, the system comprising:

Claims Text - CLTX (18):
means for capacitively coupling an electrical input through the insulator portion of the SOI structure and selectively effecting a state change to circuitry in the die; and

Claims Text - CLTX (20):
16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and circuitry in a circuit side opposite a back side, the system comprising:

Claims Text - CLTX (21):
a probe adapted to capacitively couple an electrical input through the insulator portion of the SOI structure and selectively effect a state change to circuitry in the die; and

Claims Text - CLTX (23):
17. The system of claim 16, further comprising a substrate removal arrangement adapted to remove substrate from a back side of the semiconductor die and expose the insulator portion of the SOI structure.